ABSTRACT

A phase change memory device has a semiconductor substrate; a plurality of cell arrays stacked above the ~~semiconductor~~ substrate, each cell array having a matrix of memory cells ~~arranged in a matrix manner~~ for storing resistance values as data ~~that are~~ determined by phase change of the ~~memory~~ cells, bit lines each commonly connecting one ends of plural ~~memory~~ cells arranged along a first direction of the matrix and word lines each commonly connecting the other ends of plural ~~memory~~ cells arranged along a second direction of the matrix; a read/write circuit formed on the ~~semiconductor~~ substrate as underlying the cell arrays ~~for reading and writing data of the cell arrays~~; first and second vertical wirings disposed outside of first and second boundaries ~~that define~~ of a cell layout region ~~of the cell arrays~~ in the first direction to connect the bit lines ~~of the respective cell arrays~~ to the read/write circuit; and third vertical wirings disposed outside of one of third and fourth boundaries ~~that define~~ of the cell layout region in the second direction to connect the word lines ~~of the respective cell arrays~~ to the read/write circuit.